## REMARKS

Claims 1, 2, 4, 5, 8, and 9 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated **June 4, 2003**.

### Specification

**The disclosure is objected to because of the following informalities: throughout the specification the word "fills" is spelled wrong.**

The specification has been amended, as needed, to overcome this objection. Reconsideration and withdrawal of this objection is respectfully requested.

### Claim Objections

**Claims 1-5 are objected to because of the following informalities: the numbering of the claim lines appears to be wrong.**

The claims have been amended, as needed, to overcome this objection. Reconsideration and withdrawal of this objection is respectfully requested.

### Claim Rejections under 35 USC §112

**Claims 1 and 10 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

The term pitch is used to represent a horizontal length between nearest certers of the

through holes or wires. General description of the word "pitch" is used on page 3, lines 21-24, page 5, lines 1-5, page 11, lines 12-16, and page 13, line 16 to page 15 line 9 of the written specification. Therefore, the word "pitch" may be interpreted as the narrowest center-to-center distance. This interpretation is also graphically depicted in the drawings.

Reconsideration and withdrawal of this objection is respectfully requested.

**Claim Rejections under 35 USC §102**

**Claims 1-5, 7-9, and 11-14 in so far in compliance of 35 USC §112 and as best understood by the examiner are rejected under 35 USC §102(e) as being anticipated by Kazuaki et al. (Japanese Patent No. 2002-008942).**

It should be noted that the asserted Japanese prior art reference has not been filed in the United States. Therefore, Kazuaki is not qualified to substantiate this 102(e) rejection.

This reference may be used to formulate a 102(a) rejection. To overcome the potential of a 102(a) rejection, a certified translation of 2001-329687 which has an application date of October 26, 2001 is being prepared. The certified translation of 2001-329687 will be submitted to the U.S. Patent & Trademark Office as soon as it becomes available.

Reconsideration and withdrawal of this rejection are respectfully requested.

**Claim Rejections under 35 USC §103**

**Claim 6 is rejected under 35 USC §103(a) as being unpatentable over Kazuaki.**

A certified translation of 2001-329687 which has an application date of October 26, 2001 is prepared. The certified translation of 2001-329687 is concurrently submitted to the U.S.

Patent & Trademark Office. By submitting this Declaration, independent claim 1 is believed to be patentably distinguished over the asserted prior art. All claims dependent thereon, including dependent claim 4 are also patentably distinguished over the asserted prior art.

Reconsideration and withdrawal of this rejection are respectfully requested.

**Priority**

**The Office asserted that Applicant cannot rely upon the foreign priority papers to overcome the rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55.**

A certified translation of 2001-329687 which has an application date of October 26, 2001 is prepared. The certified translation of 2001-329687 is concurrently submitted to the U.S. Patent & Trademark Office.

Reconsideration and withdrawal of this rejection are respectfully requested.

**Prior Art Indicated To Be Pertinent To The Disclosure**

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

## Conclusion

In view of the aforementioned amendments and accompanying remarks, all pending claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,
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*38834*
PATENT TRADEMARK
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION OF ACCURACY OF TRANSLATION
IN LIEU OF SWORN TRANSLATION (37 C.F.R. 1.68)



The undersigned translator, having an office at

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certifies and declares that:

(1) I am fully conversant both with the Japanese and English languages.

(2) I have translated into English Japanese Patent Application Number 2001-329687 filed in Japan on October 26, 2001. A copy of said English translation is attached hereto.

(3) The translation is, to the best of my knowledge and belief, an accurate translation from the Japanese into the English language.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the matter with which this translation is used.

Date: November 4, 2003

Keishiro Takahashi

Dr. Keishiro TAKAHASHI

PATENT OFFICE

JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application : October 26, 2001

Application Number : Japanese Patent Application No. 2001-329687

Applicant(s) : FUJITSU LIMITED

Certified on January 25, 2002

Commissioner,
Patent Office Kouzo Oikawa

Certification No. 2002-3001475

| | |
|---|---|
| [NAME OF DOCUMENT] | Patent Application |
| [DOCKET NO.] | 0140555 |
| [FILING DATE] | October 26, 2001 |
| [ADDRESSEE] | Commissioner of Patent Office |
| [I.P.C.] | H01L 25/04 |
| [TITLE OF THE INVENTION] | SEMICONDUCTOR SYSTEM-IN-PACKAGE |
| [NUMBER OF CLAIM(S)] | 10 |
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| [REPRESENTATION OF OFFICIAL FEE] | | |
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| [LIST OF SUBMITTING ARTICLES] | | |
| [Name of Article] | Specification | 1 |
| [Name of Article] | Drawings | 1 |
| [Name of Article] | Abstract | 1 |
| [General Power of Attorney No.] | 9705794 | |
| [General Power of Attorney No.] | 0109607 | |
| [Necessity of Proof] | Yes | |

[NAME OF THE DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

[CLAIMS]

[CLAIM 1] A semiconductor apparatus, comprising

a support substrate having through conductors in conformity with a first pitch,

capacitors formed above said support substrate,

a wiring layer formed above said support substrate, deriving some of said through conductors toward the above via said capacitors, having branches, and constituting wirings of a second pitch, and plural semiconductor elements disposed above said wiring layer, having terminals in conformity with the second pitch, and connected with said wiring layer via said terminals.

[CLAIM 2] A semiconductor apparatus, according to claim 1, wherein said support substrate is a Si substrate having through holes with an insulation film formed on the side walls of the holes, and said through conductors are metallic conductors filling said through holes.

[CLAIM 3] A semiconductor apparatus, according to claim 1 or 2, wherein said capacitors are de-coupling capacitors connected between power source wirings, and said wiring layer has branches between said de-coupling capacitors and said semiconductor elements.

[CLAIM 4] A semiconductor apparatus, according to one of claims 1-3, wherein said through conductors include first signal wirings; said wiring layer contains second signal wirings for deriving the first signal wirings almost vertically; and said capacitors have electrodes with a vacancy around a region where said second signal wiring is located.

[CLAIM 5] A semiconductor apparatus, according to one of claims

1-4, that further has an insulation layer disposed on said support substrate, having a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, and insulating said wiring layer and said capacitors.

[CLAIM 6] A semiconductor apparatus, according to one of claims 1-5, wherein said capacitor has a capacitor dielectric layer made of an oxide containing at least one of Ba, Sr and Ti, and a pair of capacitor electrodes disposed on both sides of the capacitor dielectric layer and containing at least partially one of Pt, Ir, Ru, Pd and their oxides.

[CLAIM 7] A semiconductor apparatus, according to one of claims 1-6, that further has a circuit board having wirings of the first pitch and connected to the lower surfaces of said through conductors.

[CLAIM 8] A semiconductor apparatus, according to one of claims 1-7, wherein said second pitch is narrower than said first pitch.

[CLAIM 9] A method of manufacturing a semiconductor apparatus, comprising

(a) the step of forming through holes at a first pitch through a support substrate,

(b) the step of forming an insulation layer on the side walls of said through holes,

(c) the step of filling the through holes formed with said insulation film, with through conductors,

(d) the step of forming capacitors connected with at least some of said through conductors, and wirings connected with said through conductors or said capacitors and having a second pitch, on said support substrate, and

(e) the step of connecting a plurality of semiconductor elements having terminals in conformity with said second pitch, on said wirings.

[claim 10] A method of manufacturing a semiconductor apparatus, according to claim 9, wherein said support substrate is a Si substrate; in said step (a), both the surfaces of the Si substrate are thermally oxidized to form silicon oxide films, and through holes are formed in such a manner that they pass from one of the silicon oxide films through the silicon substrate to reach the other silicon oxide film; in said step (b), the side walls of the through holes are thermally oxidized; and

in said step (c), a seed layer is formed on a rear surface of the other silicon oxide film; and the portions of the silicon oxide layer at the bottoms of the through holes, are removed to expose the seed layer; and a plating layer is formed in the through holes using said seed layer as seeds.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD TO WHICH THE INVENTION BELONGS]

The present invention relates to a semiconductor apparatus having plural parts packaged in one module, particularly a semiconductor apparatus having capacitors connected outside semiconductor elements for improving high frequency characteristics, and to a manufacturing method thereof.

[0002]

In this specification, in the case where plural semiconductor devices are arranged as a module to constitute a semiconductor apparatus, the respective semiconductor devices are called semiconductor elements. LSIs such as CPU are also called semiconductor elements.

[0003]

[PRIOR ART]

In recent years, the system-in-packages, in which existing

chips are combined and connected at high densities to realize desired functions, are increasingly used. Compared with the case of integrating all functions on one chip, the development period can be shortened, and the cost performance can be improved.

[0004]

Furthermore, semiconductor elements such as digital LSIs are advancing to be higher in speed and lower in power consumption. Because of the lower power consumption, the supply voltage declines. For example when the load impedance changes suddenly, the supply voltage is likely to vary. If the supply voltage varies, the semiconductor element is functionally disordered. So, the role of the decoupling capacitors for inhibiting the variation of supply voltage is important.

[0005]

Since semiconductor elements are growing to be higher in speed, the influence of high frequency ripple is increasing. It is desired that the decoupling capacitors can also efficiently absorb the high frequency ripple component.

[0006]

Because of the above, it is desired to lower the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitors. For this purpose, it is desired to minimize the wiring lengths between the semiconductor chips and the capacitors.

[0007]

In the system-in-package, for connecting decoupling capacitors or the like to semiconductor chips or circuit board, there are known such techniques as (1) resin buildup technique, (2) thick ceramic film technique and (3) thin film multilayer technique.

[0008]

(1) In the resin buildup technique, with a printed board used as the substrate, an insulation layer, passive element layer and wiring layer are built up on it, and capacitors are formed immediately below semiconductor chips and are connected by through wirings. If an organic insulation layer is used as the insulation layer, the cost can be reduced, and the process can be carried out at low temperature. Furthermore, the thermal stress caused by heat cycles after mounting can be decreased, if the difference between the passive elements and the insulation layer in thermal expansion coefficient is kept small.

[0009]

If capacitors are disposed immediately below semiconductor chips, ESL can be lowered, but the pitch of through wirings in the capacitor support is as relatively large as 50 to 200 μm. The obtained capacitances of the capacitors are hundreds of picofarads per square centimeter, and this is insufficient as decoupling capacitors at high frequency.

[0010]

(2) In the thick ceramic film technique, a low loss ceramic material is used as a substrate and an insulation layer, and a dielectric layer and a resistance layer are burned integrally. Capacitors can be formed immediately below semiconductor chips, and can be connected by through wirings. The structure is excellent in parts-accomodating capability and low in dielectric loss (tanδ). So, the transmission loss at high frequency is small.

[0011]

The obtained capacitance is tens of nanofarads per square centimeter, and the function as decoupling capacitors at high frequency is insufficient. Since the ceramics shrink in volume when burned, the dimensional dispersion becomes large. So, the through

wiring pitch in the capacitor support is as large as about 100 to 200 μm.

[0012]

(3) In the thin film multilayer technique, a low dielectric constant resin is used as an insulation layer, and silicon or glass is used as a substrate. Resistances and capacitors can be formed in the layer, and the capacitors can be connected immediately below semiconductor chips by through wirings. If the process is carried out at high temperature, capacitors having large capacitances of hundreds of nanofarads per square centimeter can be obtained.

[0013]

If a semiconductor process is used, the through wiring pitch in the support can be made as small as about 20 to 50 μm. The thermal stress caused by heat cycles after mounting can be decreased if the difference between passive elements and the insulation layer in thermal expansion coefficient is kept small.

[0014]

Semiconductor elements are growing further higher in operation speed, lower in power consumption and larger in area. The transistors and wirings in each semiconductor element become finer and finer. The number of terminals of a semiconductor element is also increasing, and the pitch between terminals is diminishing. There is a limit in narrowing the through wiring pitch in the support of decoupling capacitors in accompany with the pitch of terminals of a semiconductor element.

[0015]

If capacitors are mounted near, not immediately below, semiconductor elements, capacitors with large capacitances can be realized at low cost. However, since the wirings must be routed longer, the high frequency characteristics become worse. It becomes

difficult to install decoupling capacitors suitable for semiconductor elements acting at high speed at a frequency of more than GHz.

[0016]

[THE SUBJECT WHICH THE INVENTION IS TO SOLVE]

As described above, the system-in-package encounters a restriction in suitably connecting semiconductor elements, electronic parts such as capacitors, and a circuit board.

[0017]

An object of this invention is to provide a semiconductor apparatus, in which semiconductor elements having a narrow terminal pitch, a support having through wirings at a wider pitch, and capacitors are suitably electrically connected to realize a decoupling function with lowed inductance and large capacitance.

[0018]

Another object of this invention is to provide a system-in-package that can be adapted to finer semiconductor elements.

[0019]

A further object of this invention is to provide a semiconductor apparatus containing plural semiconductor elements to be used in such a system-in-package.

[0020]

[MEANS TO SOLVE THE SUBJECT]

From one aspect of this invention, there is provided a semiconductor apparatus, comprising a support substrate having through conductors in conformity with a first pitch, capacitors formed on or above said support substrate, a wiring layer formed on or above said support, leading some of said through wirings upwards via said capacitors, having branches and having wirings in conformity

with a second pitch, and plural semiconductor elements disposed on or above said wiring layer, having terminals in conformity with the second pitch and connected with the wiring layer via said terminals.

[0021]

From another aspect of this invention, there is provided a process for producing a semiconductor apparatus, comprising (a) the step of forming through holes at a first pitch in a support substrate, (b) the step of forming an insulation layer on side walls of said through holes, (c) the step of filling in the through holes formed with said insulation film, with through conductors, (d) the step of forming capacitors connected with at least some of said through conductors, and wirings connected with said through conductors or said capacitors and having a second pitch, on said support substrate, and (e) the step of connecting plural semiconductor elements having terminals in conformity with said second pitch, with said wirings.

[0022]

[EMBODIMENTS OF THE INVENTION]

An embodiment of this invention is described below in reference to the drawings.

[0023]

Fig. 2A shows a constitution example of a system-in-package SiP. A circuit board 50 is mounted with circuit parts 52-1 through 52-5 including plural semiconductor elements.

The semiconductor elements are, for example, an arithmetic processing unit, digital signal processor, memory, high frequency IC, input/output interface, etc. Another circuit part 53 is, for example, a SAW filter.

[0024]

On the circuit board 50, wirings are formed, and between the circuit board 50 and the semiconductor elements 52-1 through 52-5 (and circuit part 53), an intermediate laminate 51 containing capacitors and wirings is connected. A process for producing the intermediate laminate 51 containing capacitors and wirings is described below.

[0025]

As shown in Fig. 1A, for example, a 6-inch Si wafer 11 is mirror-ground to have a thickness of 300 μm, and about 0.5 μm thick silicon oxide layers 12 and 13 are formed on both sides of the wafer by thermal oxidation.

[0026]

Insulation layers such as silicon oxide layers can also be formed by low-pressure chemical vapor deposition or sputtering instead of thermal oxidation. The insulation layer should act as an etching stopper when the Si substrate is dry-etched, and is not limited to silicon oxide in material. For example, the insulation layer can be, for example, an oxynitride layer, or a laminate of an oxide layer and a nitride layer.

[0027]

As shown in Fig. 1B, a resist mask PR1 made of a photo resist material is formed on the silicon oxide layer 12. Using the resist mask PR1 as an etching mask and $CF_4$ as a main etching gas, the silicon oxide layer 12 is etched to form openings 14. The openings 14 are formed according to the pattern of through wirings to be formed. At this stage, the resist mask PR1 may be removed.

[0028]

Then, using the resist mask PR1 or the patterned silicon oxide layer 12a as an etching mask, and using $SF_6$ and $C_4F_8$ as main etching gases, dry etching is carried out for anisotropic etching of the

Si substrate 11. This etching automatically stops at the lower silicon oxide layer 13. As a result, via holes 14 through the silicone oxide layer 12a and the Si substrate 11a are formed. If the resist mask PR1 has not been removed, it is removed after completion of etching.

[0029]

As shown in Fig. 1C, the Si substrate 11a is thermally oxidized to form a silicon oxide layer 15a of about 1 μm thick in the regions where the Si surface is exposed. The portions of the silicon oxide layer 13 remaining at the bottoms of the via holes, remain to have the original thickness (about 0.5 μm). The upper and lower silicon oxide layers on the Si substrate 11a are further oxidized to become silicon oxide layers 15b and 15c having a thickness of more than about 1 μm.

[0030]

As shown in Fig. 1D, a Ti layer 16 of about 0.2 μm thick and a Pt layer 17 of about 1.0 μm thick are formed on the back surface of the substrate by sputtering. The Pt layer 17 is a seed layer for the plating to be carried out later. The Ti layer 16 is an adhesive layer for promoting the adhesion of the Pt layer 17 to the Si substrate. In the case where the seed layer has good adhesiveness, the adhesive layer may be omitted. The seed layer (and the adhesive layer) can also be formed by, for example, CVD or printing instead of sputtering.

[0031]

Wet etching using a buffered hydrofluoric acid solution as an etchant is carried out to remove the portions of the silicon oxide layer 13 at the bottoms of the via holes. In this case, the other silicon oxide layers are also etched, but they are not removed entirely but partially remain due to the difference of thickness.

[0032]

The etching with a buffered hydrofluoric acid solution is followed by wet etching using a diluted hydrofluoric acid nitric acid mixed solution as an etchant, to etch the portions of the Ti layer 16 exposed at the bottoms of the via holes. As a result, the Pt layer 17 is exposed at the bottoms of the via holes. The portions of the Ti layer are molten instantaneously when the etching starts. Even if the etchant has a nature of etching also the silicon oxide layers, the thickness of the silicon oxide layers removed while the Ti layer is etched is very limited. The silicon substrate 11a remains covered with the silicon oxide layers.

[0033]

Dry etching may also be carried out instead of wet etching. Also in this case, even if the portions of the silicon oxide layer 13 at the bottoms of the via holes, are completely removed by etching, other silicon oxide layers 15a, 15b and 15c remain at least partially.

[0034]

As a result, plural through holes can be formed in the Si substrate. At the bottoms of the through holes, the seed layer for plating is exposed, and the side walls of the through holes are covered with the insulation layer. The upper surface of the Si substrate is also covered with the insulation layer.

[0035]

As shown in Fig. 1E, electroplating is carried out to form a Pt plating layer on the Pt layer 17 in the via holes 14, for forming via conductors 18 filling or packing the via holes.

[0036]

In the case where the via holes are small in diameter, the through conductors can also be formed by CVD instead of plating. In this case, the seed layer is not especially necessary, and for example, CVD can be carried out in the state of Figs. 1B or 1C.

[0037]

As shown in Fig. 1F, the upper surface of the Si substrate is flattened or planarized by chemical machanical polishing (CMP). The upper surfaces of the through conductors 18 become flush with the upper surface of the surrounding insulation layer 15b. Similarly, CMP is carried out also for the lower surface of the Si substrate, to expose the insulation layer 15c and the through conductors 18. As a result, a support substrate S having through conductors 18 can be obtained.

[0038]

As shown in Fig. 2G, a Ti layer of about 0.1 μm thick and a Pt layer of about 0.2 μm thick are formed in this order as a lower electrode layer 20 on the surface of the support substrate S by sputtering at a substrate temperature of 400°C. A resist mask PR2 is formed on the lower electrode layer 20, and using the resist mask PR2 as a mask, the lower electrode layer 20 is patterned by milling using Ar ions. The milling can also be combined with etching. Then, the resist mask PR2 is removed.

[0039]

The lower electrode 20 has a wide area, and includes a region for allowing a wiring such as a signal wiring to pass through and a vacancy around the region. In the vacancy, a deriving electrode for the wiring is formed from the same electrode layer.

[0040]

As shown in Fig. 2H, a (Ba, Sr) $TiO_3$ (BST) thin film 21 is formed on the substrate to cover the lower electrode 20, for example, at a substrate temperature of 550°C, at an Ar gas flow rate of 80 sccm, at an $O_2$ gas flow rate of 10 sccm, at a vacuum degree of 30 m Torr, with 300 W power applied for a processing time of 1 hour. Under these conditions, a 0.2 μm thick BST dielectric film having

a dielectric constant of 500 and a dielectric loss of 2% can be obtained.

[0041]

As the material having a high dielectric constant, for example, $SrTiO_3$ or $BaTiO_3$ can also be used. It is preferred to use an oxide dielectric containing at least one of Ba, Sr and Ti and having a high dielectric constant. The dielectric film can be formed by sputtering, or also sol-gel method or CVD.

[0042]

On the dielectric film 21, a resist pattern PR3 is formed, and a buffered hydrofluoric acid solution ($NH_4F$ : HF = 6 : 1) is used for etching, to expose the surfaces of the deriving electrodes and connection areas of the capacitor electrodes. Then, the resist pattern PR 3 is removed.

[0043]

As shown in Fig. 2I, a Pt layer 22 of about 0.2 μm thick is formed by sputtering at a substrate temperature of 400°C. On the Pt layer 22, a resist pattern PR4 is formed. The Pt layer 22 is selectively removed by milling using Ar ions. As a result, an upper electrode pattern and a through conductor pattern are formed. Then, the resist pattern PR4 is removed.

[0044]

As a result, the lower electrode and the upper electrode sandwiching a BST dielectric layer form a capacitor. Furthermore, in the region free from the dielectric layer, the lower electrodes and the upper electrodes form through conductors. It is preferred that the capacitor electrodes in contact with the oxide dielectric film are made of oxidation resistant material such as Au or Pt, or such material as Pt, Ir, Ru, Pd which keep conductivity even if oxidized, or their oxides.

[0045]

As shown in Fig. 2J, a photosensitive polyimide resin layer 23 is coated to cover the upper electrodes 22. It is desirable that the polyimide has a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction. Then, the thermal stress by heat cycles after mounting can be decreased.

[0046]

The photosensitive polyimide layer 23 is selectively exposed using, for example, a reticle, and developed to remove the polyimide layer in the wiring-forming regions. The polyimide layer can also be patterned by any other method.

[0047]

As shown in Fig. 2K, a Cu layer 25 is formed by electroplating on the surface of the Pt layer exposed within the openings of the polyimide layer 23. After capacitors using an oxide dielectric layer are formed, it is preferred to use Cu as wirings. Then, as required, CMP is carried out to flatten or planarize the surface of the Cu layer 25 and the polyimide layer 23.

[0048]

As shown in Fig. 3L, a Cu layer of about 0.2 μm thick is formed as a first wiring layer 26 on the polyimde layer 23 and the deriving electrodes 25 by sputtering. The sputtering can be replaced with electroless plating or a combination of electroless plating and electroplating. A resist mask is formed, and ion milling is carried out to pattern the first wiring layer 26.

[0049]

As shown in 3M, the pattern of the first wiring layer has a pitch and line width corresponding to, for example, one halves of the pitch and line width of the through conductors 18. For example, if the through conductors have a pitch of 50 μm and a line width

of 20 μm, the pattern of the first wiring layer has a pitch of 25 μm and a line width of 10 μm.

[0050]

After patterning the first wiring layer 26, a photosensitive polyimide resin is applied to form an insulation layer 28 for insulating the first wirings 26 from each other. It is preferred that the polyimide resin has a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, like the aforesaid polyimide. In the case where the first wiring layer 26 is not flush with the polyimide layer 28, it is preferred to flatten them by CMP, etc. As a result, the first wiring layer pattern is formed.

[0051]

As shown in Fig. 3N, a connection wiring pattern 29 is formed according to the same method as described before.

[0052]

As shown in Fig. 3O, the spaces in the connection wiring pattern are filled with a polyimide layer 30 according to the same method as described before.

[0053]

As shown in Fig. 3P, a Cu layer of about 0.2 μm thick is formed as a second wiring layer 31 according to the same method as described before.

[0054]

As shown in Fig. 4Q, the second wiring layer 31 is patterned according to the same method as described before, and the spaces in the pattern is filled with a polyimide insulation layer 32 as described before. As a result, a second wiring pattern is formed.

[0055]

By repeating similar steps, a desired number of wiring layers can be formed.

[0056]

As shown in Fig. 4R, a polyimide layer is formed as a protective film 33 on the surface of the wiring layer according to the same method as described before. Openings are selectively formed in the photosensitive polyimide protective film 33 according to the same method as described before, for forming electrode-leading regions.

[0057]

As shown in Fig. 4S, a Cr layer of about 0.05 μm thick, a Ni layer of about 2 μm thick, and a Au layer of about 0.2 μm thick, in this order from the bottom, are laminated on the upper surface of the substrate, to cover the protective layer 33. The laminate is patterned to form electrode pads 35.

[0058]

A protective film 34 and electrode pads 36 are formed also on the lower surface of the substrate according to the same method described before.

[0059]

For example, Pb-5 wt% Sn solder is vapor-deposited through a metal mask on the formed electrode pads 35 and 36, and a flux is applied. They are heated and molten at 350°C, to form solder bumps 37 and 38 for connection. As a result, an intermediate laminate 51 having capacitors and wiring layers is formed.

[0060]

As shown in Fig. 4T, semiconductor elements 52 are overlaid on the intermediate laminate 51, and the bumps are molten for mounting them, to form a module. Only one semiconductor element is shown in the drawing, but as shown in Fig. 5A, plural semiconductor elements 52 are connected on the intermediate laminate 51. Then, the intermediate laminate 51 is connected on the circuit board 50. Alternatively, a module having plural circuit parts mounted on the

intermediate laminate can also be offered as a product, and the user can mount it on a circuit board.

[0061]

Fig. 5B schematically shows a portion of wirings in a module. On the circuit board 50, the intermediate laminate 51 is disposed, and on the intermediate laminate 51, circuit parts 54 including plural semiconductor elements IC1 and IC2 are disposed. In the intermediate laminate 51, there are formed through conductors PC formed in the support substrate S, vertical wirings WV connected to the through conductors PC, electrodes C1 and C2 of a capacitor connected to the vertical wirings WV, and local wirings LI1 and LI2 for connecting the semiconductor elements with each other.

[0062]

The terminal pitch of the semiconductor elements IC1 and IC2 is narrower than the terminal pitch of the circuit board 50. If it is attempted to connect the terminals of the semiconductor elements IC1 and IC2 with each other via the wirings on the circuit board 50, the wiring pitch must be once expanded. If the wirings in the intermediate laminate 51 are used, the semiconductor elements IC1 and IC2 can be connected with each other using shorter wirings without changing the wiring pitch or suppressing the expansion of the wiring pitch small.

[0063]

In the constitution shown in Fig. 4T, signal wiring TS is arranged vertically from the semiconductor element 52 to the circuit board 50. Therefore, the wiring length is short. Power wirings V and G are connected to the semiconductor 52 from the circuit board 50 via each one electrode of a capacitor. The power wirings respectively have a branch in the portion above the capacitor, to form a wiring pitch adapted to the terminal pitch of the semiconductor

element 52. The opposing capacitor electrodes form a decoupling capacitance between power wirings.

[0064]

With the above constitution, semiconductor elements having a narrow terminal pitch can be efficiently connected with a circuit board having a wide wiring pitch. Furthermore, local wirings for connecting the semiconductor elements with each other without passing through the circuit board can also be formed. Capacitors having sufficient capacitances can be formed to achieve the function of decoupling capacitors.

[0065]

The present invention has been described along one embodiment, but is not limited thereto. For example, it will be obvious for those skilled in the art, to make various modifications, improvements and combinations. Features of the present invention are described below.

[0066]

(Appendix 1) A semiconductor apparatus, comprising

a support substrate having through conductors in conformity with a first pitch,

capacitors formed above said support substrate,

a wiring layer formed above said support substrate, deriving some of said through conductors toward the above via said capacitors, having branches, and constituting wirings of a second pitch, and

plural semiconductor elements disposed above said wiring layer, having terminals in conformity with the second pitch, and connected with said wiring layer via said terminals.

[0067]

(Appendix 2) A semiconductor apparatus, according to appendix 1, wherein said support substrate is a Si substrate having through

holes with an insulation film formed on the side walls of the holes, and said through conductors are metallic conductors filling said through holes.

[0068]

(Appendix 3) A semiconductor apparatus, according to appendix 2, wherein said insulation film is a silicon oxide film formed by thermal oxidation, and said silicon substrate is also covered with a silicon oxide film on both upper and lower surfaces.

[0069]

(Appendix 4) A semiconductor apparatus, according to appendix 1 or 2, wherein said capacitors are decoupling capacitors connected between power wirings, and said wiring layer has branches between said decoupling capacitors and said semiconductor elements.

[0070]

(Appendix 5) A semiconductor apparatus, according to one of appendices 1-4, wherein said through conductors include first signal wirings; said wiring layer contains second signal wirings for deriving the first signal wirings almost vertically; and said capacitors have electrodes with a vacancy in a region where said capacitor contain said second signal wiring.

[0071]

(Appendix 6) A semiconductor apparatus, according to one of appendices 1-5, that further has an insulation layer disposed on said support substrate, having a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, and insulating said wiring layer and said capacitors.

[0072]

(Appendix 7) A semiconductor apparatus, according to one of appendices 1-6, wherein said capacitor has a capacitor dielectric layer made of an oxide containing at least one of Ba, Sr and Ti,

and a pair of capacitor electrodes disposed on both sides of the capacitor dielectric layer and containing at least partially Pt, Ir, Ru, Pd or any of their oxides.

[0073]

(Appendix 8) A semiconductor apparatus, according to appendix 1, wherein said wiring layer contains wirings connecting said plural semiconductor elements with each other.

[0074]

(Appendix 9) A semiconductor apparatus, according to one of appendices 1-8, that further has a circuit board having wirings of the first pitch and connected to the lower surfaces of said through conductors.

[0075]

(Appendix 10) A semiconductor apparatus, according to one of appendices 1-9, wherein said second pitch is narrower than said first pitch.

[0076]

(Appendix 11) A semiconductor apparatus, according to one of appendices 1-10, that further contains another circuit part connected with said wiring layer.

[0077]

(Appendix 12) A method of manufacturing a semiconductor apparatus, comprising

(a) the step of forming through holes at a first pitch in a support substrate,

(b) the step of forming an insulation layer on the side walls of said through holes,

(c) the step of filling the through holes formed with said insulation film, with through conductors,

(d) the step of forming capacitors connected with at least some

of said through conductors, and wirings connected with said through conductors or said capacitors and having a second pitch, on said support substrate, and

(e) the step of connecting plural semiconductor elements having terminals in conformity with said second pitch, on said wirings.

[0078]

(Appendix 13) A method of manufacturing a semiconductor apparatus, according to appendix 12, wherein said support substrate is a Si substrate;

in said step (a), both the surfaces of the Si substrate are thermally oxidized to form silicon oxide films, and through holes are formed in such a manner that they pass from one of the silicon oxide films through the silicon substrate to reach the other silicon oxide film;

in said step (b), the side walls of the through holes are thermally oxidized; and

in said step (c), a seed layer is formed on the rear surface of the other silicon oxide film; and the portions of the silicon oxide layer are removed at the bottoms of the through holes, to expose the seed layer; and a plating layer is formed in the through holes using said seed layer as seeds.

[0079]

(Appendix 14) A method of manufacturing a semiconductor apparatus, according to appendix 13, wherein in said step (d), a lower electrode layer is formed; lower electrode layer is patterned to form a signal wiring and an electrode with a vacancy around the signal wiring; an oxide dielectric film is formed to cover the lower electrode; the oxide dielectric film is patterned to expose the signal wiring and a connection part of the lower electrode; an upper electrode layer is formed to cover the oxide dielectric film; and upper electrode layer is patterned to form a signal wiring, a wiring for connecting

with the lower electrodes and an upper electrode with a vacancy around the wiring.

[0080]

(Appendix 15) A method of manufacturing a semiconductor apparatus, according to appendix 14, wherein in said step (d), insulation layers and wiring layers are further alternately formed to have wirings disposed at the second pitch in the wiring layers.

[0081]

(Appendix 16) A method of manufacturing a semiconductor apparatus, according to appendix 15, wherein in said step (d), a wiring layer containing the wirings for connecting plural semiconductor elements with each other is formed.

[0082]

(Appendix 17) A method of manufacturing a semiconductor apparatus, according to one of appendices 12-15, that further has the step of

(f) connecting said support substrate with a circuit board having wirings in conformity with said first pitch.

[0083]

[EFFECT OF THE INVENTION]

As described above, according to the invention, a system-in-package having decoupling capacitors with good performance can be formed.

[0084]

The wirings on or above the support substrate of the capacitors can be used to connect the semiconductor elements with each other. It becomes easy to directly connect terminals disposed at a narrow pitch with each other.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1] Sectional views showing a process for producing an

intermediate laminate as an example of the present invention.

[Fig. 2] Sectional views showing a process for producing an intermediate laminate as an example of the present invention.

[Fig. 3] Sectional views showing a process for producing an intermediate laminate as an example of the present invention.

[Fig. 4] Sectional views showing a process for producing an intermediate laminate as an example of the present invention.

[Fig. 5] A plan view and a partial sectional view schematically showing the constitution of a system-in-package

[DESCRIPTION OF THE LEGENDS]

11 Si substrate

12, 13 silicon oxide layer

14 aperture (via hole)

15 silicon oxide layer

16 Ti layer

17 Pt layer

18 through conductor (Pt)

20 lower electrode

21 BST layer

22 upper electrode

23 polyimide layer

25 deriving electrode

26 first electrode layer

28 polyimide layer

29 connecting wiring

30 polyimide layer

31 second wiring layer

32, 33 polyimide layer

35, 36 electrode pad

37, 38 solder bump

50 circuit board
51 intermediate laminate
52 semiconductor element
53 other element
54 circuit parts

[NAME OF DOCUMENT] DRAWINGS

[FIG. 1]

[FIG. 2]

[FIG. 3]

[FIG. 4]

[FIG. 5]

整理番号＝０１４０５５５ 提出日 平成１３年１０月２６日
特願2001-329687 頁: 1/ 5

【書類名】 図面
FIG.1
【図1】

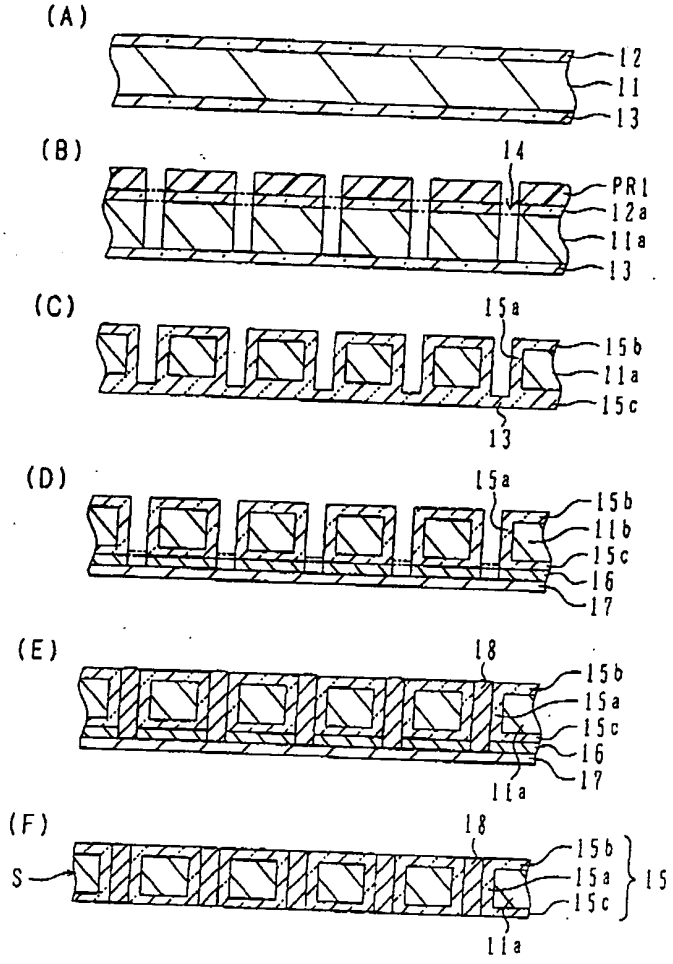
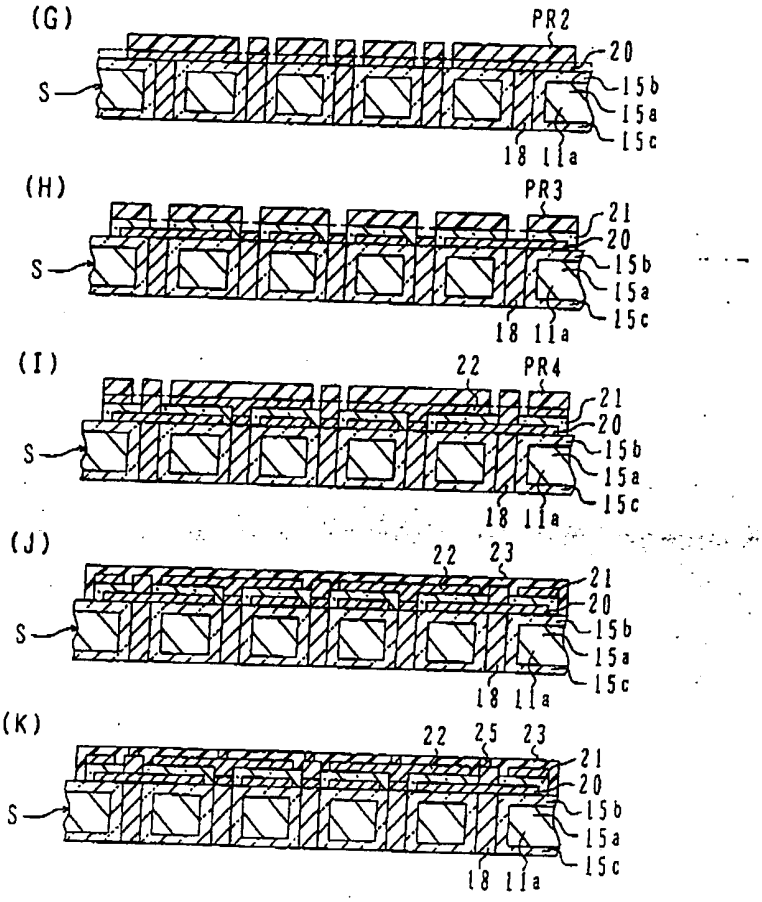


FIG. 2
[図２]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15c
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11a
(H)
PR3
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S
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18
11a
(I)
22
PR4
21
20
S
15b
15a
15c
18
11a
(J)
22
23
21
20
S
15b
15a
15c
18
11a
(K)
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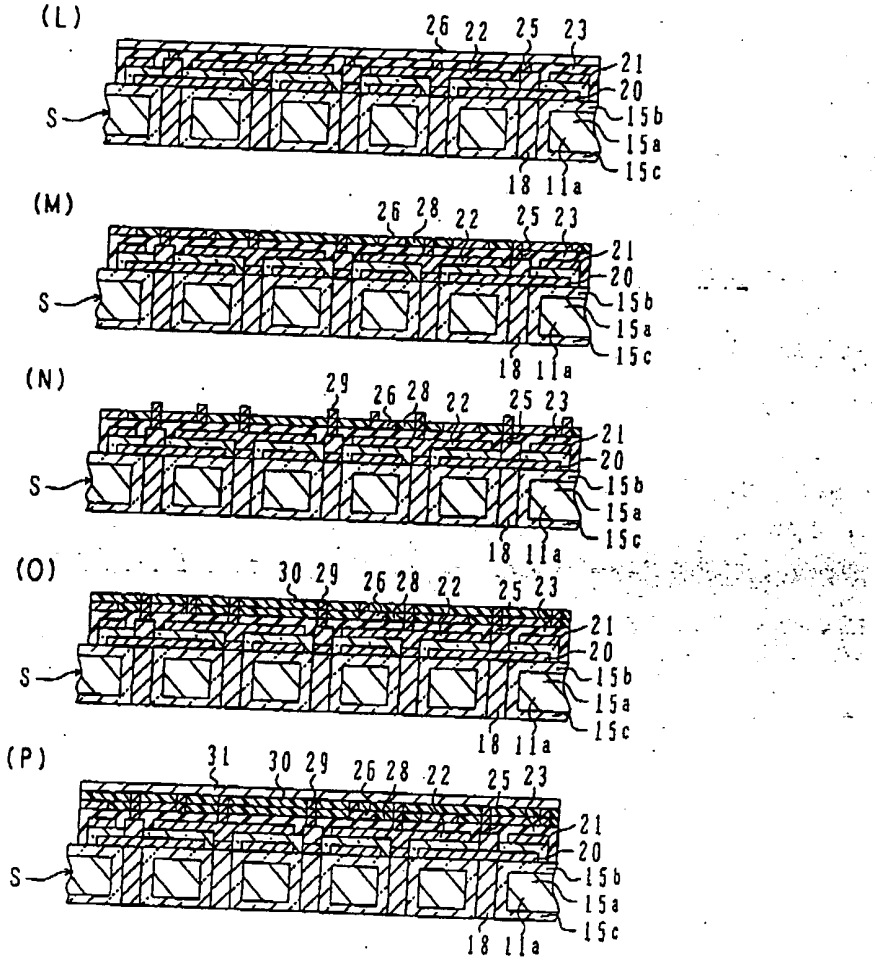
S
15b
15a
15c
18
11a

Fig. 6
【図６】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15c
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(M)
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15c
S
18 11a
(N)
29 26 28 22 25 23
21
20
15b
15a
15c
S
18 11a
(O)
30 29 26 28 22 25 23
21
20
15b
15a
15c
S
18 11a
(P)
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20
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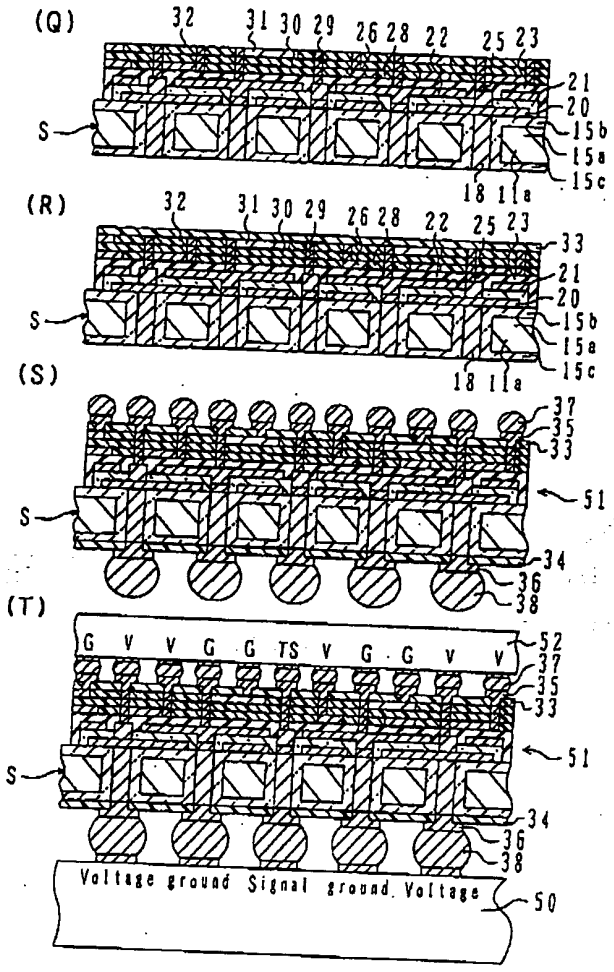
15a
15c
S
18 11a

Fig. 4
【図４】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26 28
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25 23
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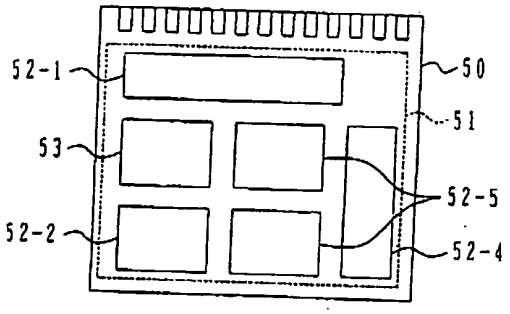
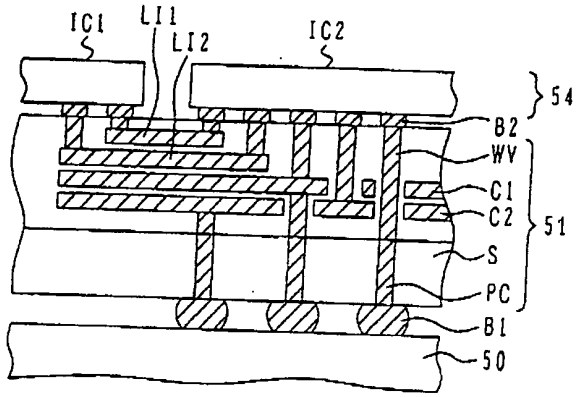
15b
15a
15c
S
18 11a
(R)
32
31 30 29
26 28
22
25 23
33
21
20
15b
15a
15c
S
18 11a
(S)
37
35
33
51
S
34
36
38
(T)
G V V G G TS V G G V V
52
37
35
33
51
S
34
36
38
Voltage ground Signal ground Voltage
50

Fig. 5
【図５】

(A)




(B)



[NAME OF THE DOCUMENT] ABSTRACT OF THE DISCLOSURE

[ABSTRACT OF THE DISCLOSURE]

[SUBJECT] A semiconductor apparatus, in which semiconductor elements having a narrow terminal pitch, a support having through wirings at a wider pitch, and capacitors are suitably electrically connected to realize the decoupling function with a large capacitance and a reduced inductance.

[SOLVING MEANS] A semiconductor apparatus comprises a support substrate having through conductors in conformity with a first pitch, capacitors formed above said support substrate, a wiring layer formed above said support substrate, deriving some of said through conductors toward the above via said capacitors, having branches, and constituting wirings of a second pitch, and plural semiconductor elements disposed above said wiring layer, having terminals in conformity with the second pitch, and connected with said wiring layer via said terminals.

[SELECTED DRAWING] FIG. 5